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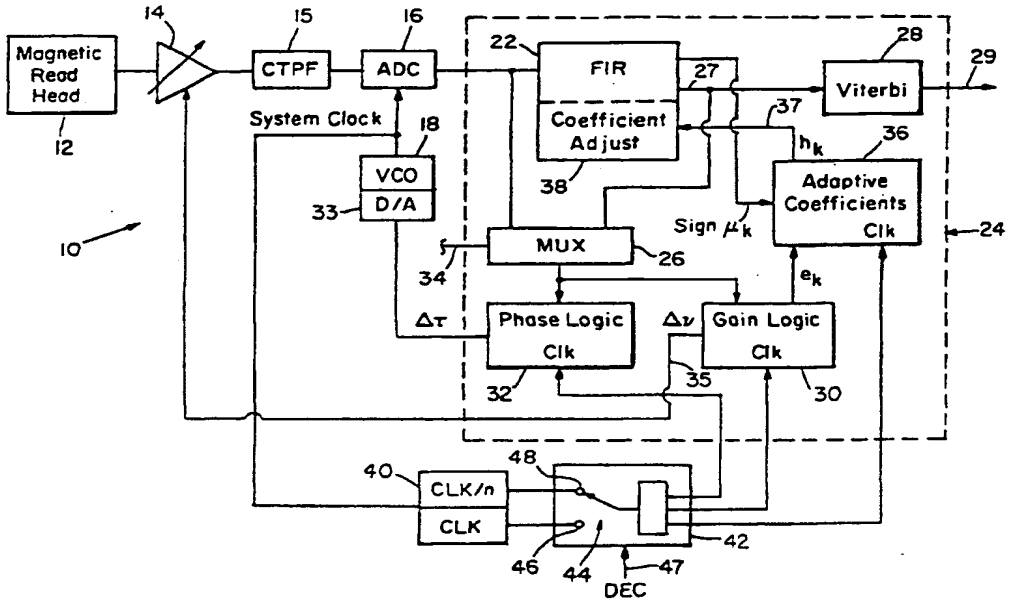


(57) Abstract

A decimating PRML signal processor system (10) for processing a PRML data signal includes: an adaptive filter circuit (22) for receiving and for shaping the data signal; a gain control circuit (30), responsive to the adaptive filter circuit (22), for adjusting the gain of the data signal; a phase control circuit (32), responsive to the adaptive filter circuit (22), for adjusting the phase of the data signal; a clock circuit (40) for providing signals for driving each of the circuits; and a decimation controller (42) for reducing the rate of the clock signals to at least one of the circuits to decrease the power required to operate the system.

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# A DECIMATING PRML SIGNAL PROCESSOR SYSTEM

## FIELD OF INVENTION

This invention relates to a partial response maximum likelihood (PRML) channel signal processor and more particularly to such a signal processor which has reduced power requirements.

## BACKGROUND OF INVENTION

In magnetic recording devices, such as magnetic disks and tapes, a recording head is used to read and write information to and from a magnetic surface. In a typical rotating-based storage system, data is stored on magnetic disks in a series of tracks. The read/write head detects variations in the magnetic orientation of the disk surface. A pattern of external and internal fields are created as the head and recording surface are moved relative to each other. The patterns are similar to a series of bar magnetics of changing polarities. The polarity transitions are then readable as transitions in the magnetic flux at the recording surface. In the read mode the magnetic field of the storage surface is detected and a voltage is induced in a coil proportional to the rate of change of the flux. Read channels, such as partial response maximum likelihood (PRML) channels, then process this analog voltage signal to obtain the digital data. PRML channels typically include, *inter alia*, an analog to digital converter (ADC) which converts incoming analog data signals from a storage medium to digital signals and a digital signal processor system which is comprised of a timing recovery loop, gain recovery loop and an adaptive filter circuit. The adaptive filter circuit shapes the data signal so that it conforms to the typical shape of the PRML signal to be detected. The timing recovery loop, also known as the phase control loop, adjusts the sampling phase of the data signal provided to the ADC and the gain recovery or control loop adjusts the gain of the data signal provided to the ADC.

The adaptive filter, timing recovery loop, and gain

recovery loop are complex circuits which contain, among other things, many banks of delay registers. In typical PRML channels the adaptive filter, timing recovery and gain recovery loops operate at the same frequency as the sampling clock which samples the incoming data signals so that each time the data signals are sampled all of the capacitors within the banks of registers are charged. It is known that the power dissipated in these circuits is proportional to the operating frequency of the circuits. Thus, since the clock sampling frequency which operates these circuits is very high, typically 125 MHz, the digital signal processing circuit and hence the PRML channel have significant power requirements.

## SUMMARY OF INVENTION

It is therefore an object of this invention to provide a PRML signal processor system with reduced power requirements.

It is a further object of this invention to provide such a PRML signal processor system which selectively decimates the operating frequency of one or more of the adaptive filter, timing recovery and gain recovery loops to reduce the power consumed by the PRML channel.

This invention results from the realization that the power requirements of a PRML signal processor system and PRML channel are directly proportional to the operating frequency of its circuits and from the further realization that a truly power efficient PRML signal processor system and channel can be achieved by decreasing or decimating the frequency of operation of one or more of the adaptive filter, timing recovery loop and gain recovery loop. This invention features a decimating PRML signal processor system for processing a PRML data signal which includes an adaptive filter circuit for receiving and shaping the data signal. There are a gain control circuit and a phase control circuit, both responsive to the adaptive filter, for adjusting the gain of the data signal and the phase of the data signal, respectively. There is a clock circuit for providing clock signals for driving each of the circuits and a decimation controller for reducing

the rate of the clock signals to at least one of the circuits to decrease the power required to operate the system.

In a preferred embodiment there may further be included an analog to digital converter for converting the data signal from analog to digital and providing the digital signal to the adaptive filter circuit. The controller may include means for reducing the clock rate at the same level for each circuit. The controller may include means for reducing the clock rate at different levels for each circuit. The phase control circuit may include a mode selector for setting the phase control circuit to one of a tracking mode and an acquisition training mode. The mode selector may interconnect the phase control circuit with the adaptive filter in the tracking mode and to the ADC in the acquisition training mode.

## DISCLOSURE OF PREFERRED EMBODIMENT

Other objects, features and advantages will occur to those skilled in the art from the following description of a preferred embodiment and the accompanying drawings, in which:

Fig. 1 is a schematic block diagram of the decimating PRML signal processor system according to this invention;

Fig. 1A is a more detailed schematic block diagram of the decimation controller of Fig. 1;

Fig. 2 is an analog PRML waveform illustrating the function of the phase control circuit of Fig. 1;

Fig. 3 is a schematic diagram of the input registers of a prior art phase control circuit;

Fig. 4 is a timing diagram depicting the operation of the prior art phase control circuit of Fig. 3;

Fig. 5 is a schematic diagram of the input registers of the phase control circuit of Fig. 1 according to this invention;

Fig. 6 is a timing diagram of the phase control circuit of Fig. 5;

Fig. 7 illustrates the operation of the gain control circuit of Fig. 1;

Fig. 8 is a schematic diagram of the input circuit of a

prior art data control circuit;

Fig. 9 is a timing diagram of the prior art gain control circuit of Fig. 8;

Fig. 10 is schematic diagram of the gain control circuit of Fig. 1 according to this invention;

Fig. 11 is a timing diagram of the gain control circuit of Fig. 10;

Fig. 12 depicts a data signal waveform and a standard PRML waveform illustrating the operation of the adaptive filter circuit;

Fig. 13 is a schematic diagram of a prior art adaptive coefficient circuit;

Fig. 14 is a timing diagram of the prior art circuit of Fig. 13;

Fig. 15 is a schematic diagram of the adaptive coefficient circuit of Fig. 1 according to this invention; and

Fig. 16 is a timing diagram of the adaptive coefficient circuit of Fig. 15.

There is shown in Fig. 1 a partial response maximum likelihood (PRML) channel 10 for processing a read signal from a storage medium obtained by magnetic read head 12. Magnetic read head 12 provides data signals read from the storage medium to a variable gain amplifier 14 which outputs the data signals to continuous time programmable filter 15. Continuous time programmable filter 15 converts the incoming raw analog read signals to analog PRML signals of a predetermined order (e.g. PR4, EPR4). The PRML signals from continuous time programmable filter 15 are provided to analog to digital converter (ADC) 16 which samples the analog PRML signals at the system clock frequency, typically, 125 MHz, which clock signal is provided by a system sampling clock within voltage controlled oscillator (VCO) 18. Digital signals sampled at the clock frequency are provided from analog to digital converter 16 to finite impulse response (FIR) filter 22 within digital signal processing block 24 and to multiplexer 26 whose function is described below. FIR filter 22 outputs over line 27 a multi-level PRML digital signal to Viterbi detector 28

which decodes the signal and outputs over line 29 a serial binary signal corresponding to the analog signals read by magnetic read head 12 from the storage disk. The output of FIR filter 22 over line 27 is also provided to multiplexer 26. The output of multiplexer 26 is provided to gain control circuit 30 and phase control circuit 32.

Phase control circuit 32 provides phase error feedback signals $\Delta r$ to digital to analog converter 33 which causes VCO 18 to adjust the sampling phase of ADC 16 to ensure that the analog read signals are being sampled appropriately. This phase control technique is well known in the art and is often referred to as phase or timing recovery. See for example, U.S. Patent No. 4,890,299, entitled Fast Timing Acquisition for Partial-Response Signalling, issued December 26, 1989 and No. 5,341,249, entitled Disk Drive Using PRML Class IV Sampling Data Detection with Adaptive Equalization, issued August 23, 1994 both of which are incorporated herein by reference in their entireties. See also Cideciyan et al., "A PRML System for Digital Magnetic Recording", IEEE Journal in Selected Areas in Communications, Vol. 10, No. 1, January 1992, Pgs. 38-56, incorporated herein by reference in its entirety.

During normal operation, in the tracking mode, multiplexer 26 selects the signal from line 27 at the output of FIR filter 22 as the input to phase control circuit 32 in response to a signal on line 34 to multiplexer 26. However, each time PRML channel 10 is initially utilized a signal is provided over line 34 to multiplexer 26 which causes multiplexer 26 to provide phase control circuit 32 with the output of analog to digital converter 16. The signal enabling this selection of multiplexer 26 is typically called the acquisition signal and when this signal is used, the phase recovery loop is referred to as the acquisition phase recovery loop. This acquisition recovery loop is used to shorten the phase correction by locking to the phase of the preamble signal which closely matches the phase of the data signals to be read in the tracking mode. Then, the signal over line 34

causes multiplexer 26 to switch to the normal tracking mode.

Gain control circuit 30 provides a gain error feedback signal $\Delta\nu$ over line 35 to variable gain amplifier 14 to adjust the gain of the data signal so that its amplitude matches the amplitude of the predetermined PRML signal which is programmed by the user. The gain control technique is well known in the art. See, for example, U.S. Patent Nos. 4,890,299 and 5,341,249 and the publication "A PRML System for Digital Magnetic Recording".

Adaptive coefficient circuit block 36 receives from gain control circuit 30 a gain error signal, $e_k$, which is used to calculate $\Delta\nu$ within gain control circuit 30, and a slope signal, sign $\mu_k$, from FIR filter 22. From these input signals, as described below, the adaptive coefficients, $h_k$, are calculated and are provided over line 37 to coefficient adjust circuit 38 within FIR filter 22. Within FIR circuit 22, as is well known in the art, are a number of multipliers which adjust the output of FIR filter 22 according to the values of coefficients $h_k$ in order to shape the FIR filter output signal in accordance with the desired PRML signal. See, for example, U.S. Patent No. 5,341,249 and publication "A PRML System for Digital Magnetic Recording". Thus, the adaptive coefficient circuit block 36 and the coefficient circuit 38 of FIR filter 22 form in conjunction an adaptive filter circuit.

Phase control circuit 32, gain control circuit 30 and adaptive coefficient circuit 36 all operate under the control of a clock signal. In prior art systems these circuits operate under the control of the system clock, which controls the sampling frequency of the analog to digital converter 16. This system clock, however, operates at a very high frequency, typically 125 MHz. The amount of power dissipated in each of these circuits may be expressed as follows:

$$P=fCV^2 \qquad (1)$$

Where P is equal to the power dissipated in each circuit, f is the frequency of operation of the circuit, C is the total driven capacitance of the circuit, and V is the supply voltage

of the circuit. Since the capacitance and voltage are essentially fixed for these circuits which, as described in the Background of Invention, contain a large number of delay registers that require charging at each sample time, the instant inventors realized that by reducing the frequency of operation of these circuits the power dissipated by each circuit and hence by the overall PRML channel can be reduced.

Adjustable clock frequency circuit 40, which receives the system clock frequency from VCO 18, is capable of outputting the system clock frequency and virtually any (n) multiple of the system clock frequency to gain and phase control circuits 30 and 32 and adaptive coefficient circuit 36 to reduce the power dissipated by these circuits, digital signal processor circuit 24, and the overall PRML channel 10.

This is accomplished by decimation controller 42 which includes a switch 44 (actually comprised of three individual switches as shown in Fig. 1A) that when switched into connection with terminal 46, under the control of a decimation control signal over line 47, is exclusively in connection with the system clock. In this position gain control circuit 30, phase control circuit 32, and adaptive coefficient circuit 36 are all operated in accordance with prior art systems at the system clock sampling frequency. However, when switch 44 is switched into connection with terminal 48, reduced frequency clock 40, is capable of operating all three of the gain control circuit 30, phase control circuit 32 and adaptive coefficient circuit 36 at reduced frequencies to reduce the power dissipated in these circuits. Or, each of these circuits can be operated at the same reduced frequency, each at a different reduced frequency, or two at one reduced frequency and the other at another reduced frequency. Circuit 40 is even capable of operating any one or two of the circuits at the system clock frequency and one or two of the others at a reduced frequency.

Decimation controller 42 is shown in more detail in Fig. 1A to include three individual switches 44a-c, interconnected at a first end with phase control circuit 32, gain control

circuit 30 and adaptive coefficient circuit 36, respectively, and at a second end selectively interconnected with terminals 46a-c or terminals 48a-c. The positions of switches 44a-c are individually controlled by control signals supplied over lines 47a-c. Terminals 48a-c include a number of sub terminals, such as 48a'-48c', which enable the interconnection of the switches to various reduced frequency clock signals CK/2...CK/n. As described in detail below, this invention, which reduces the amount of power consumed by phase control circuit 32, gain control circuit 30 and adaptive coefficient circuit 36, is achieved by operating each of these circuits with two clock signals, $CK_1$ and $CK_2$, having an increased period (or reduced frequency) which is a multiple of the system clock period, wherein clock signal $CK_2$ is delayed by one system clock period with respect to clock signal $CK_1$. Thus, reduced clock circuit 40 generates pairs of reduced frequency clock signals ($CK_1$ and $CK_2$) at frequencies CK/2...CK/n and these signals are provided to terminals 48a-48c. Also, system clock signals CK are provided to terminals 46a-c. Therefore, switches 44a-c can be individually connected to any pair of reduced frequency clock signals or to the pair of system clock signals to operate each circuit individually at either a reduced frequency or at the system clock frequency, respectively.

The effect of being able to operate these circuits at a reduced frequency is a reduction in power required by the digital signal processor circuit 24 and the overall PRML channel 10. Clock logic circuit is typically programmed to operate the circuits at predetermined frequency but the operating frequencies of the circuits may be adjusted by the user.

The function of phase control circuit 32, gain control circuit 30, and adaptive coefficient circuit 36, the previous design of their input registers, and the design of their input registers according to this invention is described in turn below. Although the PRML waveforms described below are PR4 waveforms this is not a limitation of this invention as other order PRML signals could also be utilized. Moreover, the

invention is described below using clock frequencies reduced by 50% (i.e. CK/2) and this is also not a limitation of this invention as any reduced frequency which is a multiple of the system clock frequency may be utilized as long as the circuits still properly perform their function.

PHASE CONTROL CIRCUIT

Analog PRML waveform 50, Fig. 2, transformed by continuous time programmable filter 15 into a PR4 signal, is input to analog to digital converter 16, Fig. 1, and is sampled a number of times as indicated by sample points 52 $D_0$, 53 $D_1$, 54 $D_2$, 55 $D_3$, 56 $D_4$ and 57 $D_5$. Phase control circuit 32 compares adjacent samples taking proper account of sign, such as 52 $D_0$ and 53 $D_1$ to see if they are equal. If they are equal then this indicates that the sampling frequency is in phase with waveform 50 and is sampling the PR4 signal properly at points located symmetrically about peak 60. However, in this example, sample point 53 $D_1$ has a value of nineteen, (twenty-four corresponds to peak value 60), while sample point 52 $D_0$ has a value of twenty. This indicates that for proper sampling sample $D_1$ should actually be taken at sample point 53' with a value equivalent to twenty. Therefore, the sampling frequency is adjusted accordingly by a phase error signal $\Delta\tau$ generated by phase control circuit 32. With prior art PRML signal processor systems each pair of sample points are compared and are used to generate phase error signal $\Delta\tau$. That is, signals 52 $D_0$ and 53 $D_1$, 53 $D_1$ and 54 $D_2$, 54 $D_2$ and 55 $D_3$, 55 $D_3$ and 56 $D_4$ and 56 $D_4$ and 57 $D_5$...etc. are compared and used to generate phase error signal $\Delta\tau$.

Phase control circuit 32', configured according to prior art systems to operate exclusively at the system clock sampling frequency, is shown in Fig. 3 to include a set of input registers 70 and 72, for generating the $Y_{(n)}$ (sign $Y_{(n)}$) and $Y_{(n-1)}$ (sign $Y_{(n-1)}$) signals on output lines 74 and 76, respectively, from input signal $D_n$ on input line 78. Signal Dn is actually the output in the tracking mode from FIR filter

22, Fig. 1, provided over line 27. The sign signals are simply the most significant bits of the samples. Signal $Y_{(n)}$ is the present sample $D_n$ output from delay register 70 and sign $(Y_{(n)})$ is the polarity (+ or −) of that sample. Signal $Y_{(n-1)}$ is the previous sample $D_{(n-1)}$ which was delayed by delay register 72 and sign $(Y_{(n-1)})$ is the polarity of that sample. These delay registers and the remaining circuitry in phase control circuit 32' operate under the control of the system clock frequency by a clock signal supplied on input line 82 tied to both delay registers 70 and 72 which causes signals $Y_{(n)}$ (sign $Y_{(n)}$) and $Y_{(n-1)}$ (sign $(Y_{(n-1)})$ to be generated every clock cycle. There signals are used to calculate the phase error signal $\Delta\tau$ according to the following equation:

$$\Delta\tau = -y_n * sgn(y_{n-1}) + y_{n-1} * sgn(y_n) \qquad (2)$$

Timing diagram 90, Fig. 4, depicts how the incoming samples $D_0$ - $D_5$, Fig. 2, to phase control circuit 32', Fig. 3, are used to calculate a phase error signal $\Delta\tau$ every cycle of the system sample clock. Signals $D_0$ - $D_5$ of waveform 92 are typically 6 bit digital words representing the values of samples of data from waveform 50, Fig. 2, which are provided to phase control circuit 32' at the system clock sample rate shown in waveform 94. Waveform 96 depicts the $Y_{(n)}$ (sign $Y_{(n)}$) output on line 74, Fig. 3, after each clock cycle and waveform 98 depicts the $Y_{(n-1)}$ (sign $Y_{(n-1)}$) output on line 76, Fig. 3, which is delayed one clock cycle from the waveform 96. That is, for example, when $Y_{(n)}$ is $D_1$, $Y_{(n-1)}$ is $D_0$. Waveform 100 illustrates that the phase error signal $\Delta\tau$ is generated at every clock cycle and it is generated for each adjacent sample (i.e. $D_0$ and $D_1$, $D_1$ and $D_2$, $D_2$ and $D_3$, $D_3$ and $D_4$, and $D_4$ and $D_5$).

Phase control circuit 32, Fig. 5, according to this invention is shown to include a set of input registers 110 and 112 whose operation is controlled by separate clock signals $CK_1$ and $CK_2$ on input lines 114 and 116 with frequencies lower than the system clock sampling frequency CK and delayed one system

clock period with respect to each other. Input signal $D_n$ is introduced to both delay registers 110 and 112 on input line 118, output signals $Y_{(n)}$ (sign $(Y_{(n)})$ are output from delay register 112 over line 120 and signals $Y_{(n-1)}$ (sign $(Y_{(n-1)})$ are output from delay register 110 over output line 122.

Timing diagram 130, Fig. 6, illustrates the timing of clock signals $CK_1$ and $CK_2$ according to this invention and how they effect the outputs of delay registers 110 and 112, Fig. 5 as well as the error signal outputs $\Delta\tau$ from phase control circuit 32. Sample data waveform 132 including samples $D_0$ - $D_5$, Fig 2, is sampled at the system clock frequency depicted by waveform 134. However, because phase control circuit 32, Fig. 5, is operated at a reduced frequency it does not utilize each data sample $D_0$ - $D_5$ in calculating the phase error signal $\Delta\tau$. Delay register 110, Fig. 5, is operated by clock signals $CK_1$, waveform 136, and delay register 112, Fig. 5, is operated by clock signals $CK_2$, waveform 138. In this example, clock signals $CK_1$ and $CK_2$ operate at one half the system clock sampling frequency and are offset in time from each other by one period of the system clock. Because the clock frequency operating phase control circuit 32 is effectively reduced or decimated by 50%, the update rate of the phase error calculations is similarly reduced. That is, because of clock signals $CK_1$ and $CK_2$ outputs of delay registers 112, $Y_{(n)}$ (sign $(Y_{(n)})$, and 110, $Y_{(n-1)}$ (sign $(Y_{(n-1)})$, see only every other sample. Output 110 sees only samples $D_1$, $D_3$ and $D_5$, waveform 140, while output 112, waveform 142, sees samples $D_0$, $D_2$ and $D_4$. The result of this is that phase error signal $\Delta\tau$ is calculated only 50% of the time. As illustrated by waveform 144 $\Delta\tau$ signals generated only by sample pairs $D_0$ and $D_1$, $D_2$ and $D_3$, and $D_4$ and $D_5$ are calculated. Since, in this example, the frequency of operation of phase control circuit 32 is reduced by 50%, so is the power consumed by the circuit.

GAIN CONTROL CIRCUIT

The operation of the gain control circuit 30, Fig. 1, is

best illustrated by observing waveforms 150 and 152, Fig. 7, which represent, respectively, the actual analog data signal introduced to analog to digital converter 16 and a desired analog data read signal during preamble. Gain control circuit 30 is used to provide a feedback error correction signal $\Delta v$ to variable gain amplifier 14 to adjust waveform 150 so that its amplitude at the various sample points, taken at the system clock sampling frequency, are equivalent to the amplitude of the desired analog PRML waveform 152. Sample points 153 $YY_1$, 154 $YY_2$, 155 $YY_3$, 156 $YY_4$ and 157 $YY_5$ are shown not to coincide with desired sample points 153'-157'. Thus, gain control circuit 30 accordingly adjusts variable gain amplifier 14 with an error correction signal $\Delta v$ to amplify waveform 150 such that it has the desired amplitude.

Prior art gain control circuit 30', configured according to prior art systems to operate exclusively at the system clock sampling frequency, is shown in Fig. 8 to include an input circuit 160 which includes input registers 162 and 164 and gain logic circuit 166. Signal $YY_n$ (sign $YY_n$) is input to delay register 162 over input line 168. The output of delay register 162 is the delayed sample $YY_n'$ (sign $YY_n'$), which is input to gain logic circuit 166. Gain logic circuit 166 calculates signal gain error signal $e_k$ and provides that signal to delay register 164 which outputs on line 170 the $e_k$ error signal. Input registers 162 and 164 are operated by the system clock supplied over line 172. Within gain control circuit 30' the following gain error algorithm is implemented using error signal $e_k$ to generate the gain error correction signal $\Delta v$:

$$\Delta v = sign(YY_n)\,|e_k| \qquad (3)$$

Timing diagram 200, Fig. 9, depicts the timing of obtaining samples $YY_n$, (sign $YY_n'$) and the calculation of error signal $e_k$ and gain error correction signal $\Delta v$. Sample waveform 202 which is output from FIR filter 22, Fig. 1, includes an

output of digital 6 bit samples $YY_1 \ldots YY_5$ taken at the system clock sampling frequency which is depicted by waveform 204. Waveform 206 shows that error signals $e_{k1} \ldots e_{k4}$ are obtained at the onset of each clock signal and used in the calculation of the gain error correction signal $\Delta\nu$, waveform 207, at each clock cycle. It can be seen that between the time that each sample $YY_n$ is obtained and the error signal $e_{km}$ is output, there is a delay of one clock signal. For example, at clock signal 208 data sample $YY_1$ (sign $YY_1$) 210 is obtained, but not until clock signal 212 is signal $e_{k1}$ 214 output and used to calculate gain error correction signal $\Delta\nu$.

Gain control circuit 30, Fig. 10, is configured according to the present invention to operate at a fraction of the normal clock sample rate. Circuit 30 includes input delay registers 220 and 222 with gain logic circuit 224 interconnected therebetween. Signal $YY_n$ (sign $YY_n$) is input to delay register 220 over line 226 at the first clock signal $CK_1$ supplied over line 228. Delay registers 220 outputs a delayed signal $YY_n'$ (sign $YY_n'$) to gain logic 224 which outputs error signal $e_k$ to delay register 222 driven by a second clock signal $CK_2$ supplied over line 230. Delay register 222 outputs over line 232 the gain error correction signal $\Delta\nu$ provided to variable gain amplifier 14, Fig. 1. Clock signals $CK_1$, $CK_2$ are operated at a fraction of the system clock sampling frequency which, as demonstrated below, reduces the update rate of the gain error calculations and hence the power consumed by gain control circuit 30.

Timing diagram 240, Fig. 11, illustrates how using the present invention which reduces or decimates the clock signal operating gain control circuit 30 does not utilize all of the sample data output from the FIR filter 22 to generate the error correction signal $\Delta\nu$. In this example, samples used in calculating $\Delta\nu$ are taken at one half the normal frequency or rate, thereby reducing the power consumed by gain circuit 30 by one half. Data signal waveform 242 includes a number of 6 bit data samples $YY_0$ - $YY_5$ which are output from FIR filter 22,

Fig. 1, at the system clock frequency shown by waveform 244. Clock waveforms $CK_1$ 246 and $CK_2$ 248 which, in this example, operate at one half the system clock frequency, are delayed relative to one another by one clock period of waveform 244. These clock signals $CK_1$ and $CK_2$ respectively operate delay registers 220 and 222 of Fig. 10. Clock signal $CK_1$ is used to cause delayed sample $YY_n'$ to be output from delay register 220, Fig. 10, at the rising edge of each $CK_1$ clock signal and to generate the error signal $e_k$ corresponding to sample $YY_n$ as indicated by waveform 250. Since this frequency is half of the system clock frequency, (waveform 244) only every other data sample, in this case $YY_0$, $YY_2$, are $YY_4$ are obtained by gain control circuit 30. Waveform 252 illustrates that at the leading edge of every $CK_2$ clock signal, the gain error correction signal $\Delta\nu$ for each sample ($YY_0$, $YY_2$, and $YY_4$) is calculated and generated. Because delay registers 220, 222 are operated at half the clock frequency only half the samples taken by analog to digital converter 16, Fig. 1, are used by the gain control circuit 30 to calculate and generate a gain error correction signal $\Delta\nu$, thus, decreasing the amount of power required to operate gain control circuit 30 by one half.

ADAPTIVE FILTERING

Analog PRML waveform 260, Fig. 12, is sampled at sample points 262 $D_0$, 263 $D_1$, 264 $D_2$, 265 $D_3$, 266 $D_4$ and 267 $D_5$. The gain and phase control circuits are used to adjust the sampling phase to ensure that sampling is occurring at the proper portion of the incoming PRML waveform and that the gain of the incoming PRML waveform is at the appropriate level, respectively. Adaptive filtering operates to shape the PRML incoming waveform so that it conforms to the shape of a predetermined PRML waveform indicated by waveform 270. Because waveform 260 at, for example, sample points 262, 263, and 264 does not agree with samples 272', 273 ' and 274' it does not conform to the expected PRML wave shape. Thus, as described below, adaptive coefficients within adaptive

coefficient circuit 36, Fig. 1, are generated and output to coefficient update adjust circuit 38 within FIR filter 22 to adjust the output of FIR filter 22 so that its output waveform does correspond to the expected PRML wave shape.

Prior art adaptive coefficient circuit 36', Fig. 13, configured to operate exclusively at the system clock frequency, includes a set of input registers 280 and 282 which receive, respectively, error signal, $e_k$, and slope signal, sign $u_k$, from gain control circuit 30 and FIR filter 22, respectively. These delay registers are driven by the system clock signals over line 284 and after each delay period both signals are supplied to system logic 286 which calculates the adaptive coefficients $h_k$ according to the following formula:

$$h_k = h_{k-1} + \beta e_k sign u_k \quad (4)$$

where $h_k$ are the new coefficients, $h_{k-1}$ are the previous coefficients, $\beta$ is the loop gain, $e_k$ is the error signal from gain control circuit 30 and sign $u_k$ is the slope signal from FIR filter 22. The $h_{k+1}$ adaptive coefficients from logic 286 are supplied to delay register 288 which, after a delay, supplies the adaptive coefficients $h_k$ over line 290 to coefficient adjust circuit 38 within FIR filter 22 to provide appropriate shaping of the waveform.

Timing diagram 300, Fig. 14, depicts how the $e_k$ and sign $u_k$ data samples are generated each system clock cycle as indicated by waveform 302. System clock waveform 304 shows that at the leading edge of each clock signal, the $e_k$ and sign $u_k$ samples are taken. Adaptive coefficient waveform 306 depicts that at the leading edge of each clock signal following the signal cycle which obtained the $e_k$ and sign $u_k$ data samples the $h_{k+1}$ coefficients are generated and output. The updated coefficients, $h_k$, are available one clock cycle later over line 290 as indicated by waveform 307. With prior art adaptive coefficient circuit 36' adaptive coefficients $h_{k0}...h_{k5}$ are calculated for each pair of data samples $e_{k0}$, sign $u_{k0}$ - $e_{k5}$, sign $e_{k5}$. Thus, the frequency of operation of the

adaptive coefficient circuit corresponds to the system sampling frequency.

With the present invention adaptive coefficient circuit 36 includes input registers 310 and 312 driven by a reduced clock frequency signal $CK_1$ provided over line 314. Delay registers 310 and 312 provide to logic circuit 316 the $e_k$ and sign $u_k$ signals from gain control circuit 30 and FIR filter 22, Fig. 1, respectively. Delay register 318, however, is driven by a second clock signal $CK_2$, provided over line 319, operating at the same reduced frequency as $CK_1$ except it is delayed relative to $CK_1$ by the equivalent of one normal clock period of CK waveform 304, Fig. 14.

Timing diagram 320, Fig. 16, depicts how adaptive coefficients $h_k$ are output less often with circuit 36, Fig. 15, than with circuit 36', Fig. 13. Waveform 322 depicts data signals $e_{k0}$ and $signU_{k0}$ - $ek_5$ and $signU_{k5}$. Clock $CK_1$ waveform 326 operates, in this example, at one half of the system clock frequency depicted as waveform 324. At the leading edge of each pulse of $CK_1$ clock waveform 326 data samples $e_k$ and sign $u_k$ are output from delay registers 310 and 312. As illustrated by waveform 330 only every other data sample, i.e. $e_{k1}$ (sign $u_{k1}$), $e_{k3}$ (sign $u_{k3}$), and...$e_{k5}$ (sign $u_{k5}$) is utilized. Clock waveform $CK_2$ 328 is used for timing the output of the adaptive coefficients $h_k$. At each leading edge of the pulses of waveform 328 the adaptive coefficients $h_k$ are generated, waveform 332. Because only every other data sample is utilized, only the adaptive coefficients $h_k$ for every other data sample are output thereby reducing the power consumed by 50% as compared to prior art adaptive coefficient circuit 36, Fig. 13.

Each of the circuits 30, 32 and 36 could by operated at the system clock frequency by providing the system clock signals to both the $CK_1$ and $CK_2$ inputs of these circuits.

Although specific features of this invention are shown in some drawings and not others, this is for convenience only as each feature may be combined with any or all of the other

features in accordance with the invention.

Other embodiments will occur to those skilled in the art and are within the following claims:

## CLAIMS

1. A decimating PRML signal processor system for processing a PRML data signal comprising:

an adaptive filter circuit for receiving and shaping the data signal;

a gain control circuit, responsive to said adaptive filter circuit, for adjusting the phase of said data signal;

a phase control circuit, responsive to said adaptive filter circuit, for adjusting the phase of said data signal;

a clock circuit for providing clock signals for driving each of said circuits; and

a decimation controller for reducing the rate of said clock signals to at least one of said circuits to decrease the power required to operate the system.

2. The decimating PRML signal processor system of claim 1 further including an analog to digital converter for converting said data signal from analog to digital and providing said digital signal to said adaptive filter circuit.

3. The decimating PRML signal processor system of claim 1 in which said controller includes means for reducing the clock rate at the same level for each circuit.

4. The decimating PRML signal processor system of claim 1 in which said controller includes means for reducing the clock rate at different levels for each circuit.

5. The decimating PRML signal processor system of claim 1 in which said phase control circuit includes a mode selector for setting said phase control circuit to one of a tracking mode and an acquisition training mode.

6. The decimating PRML signal processor system of claim 5 in which said mode selector interconnects said phase

control circuit with said adaptive filter in said tracking mode and to said ADC in said acquisition training mode.

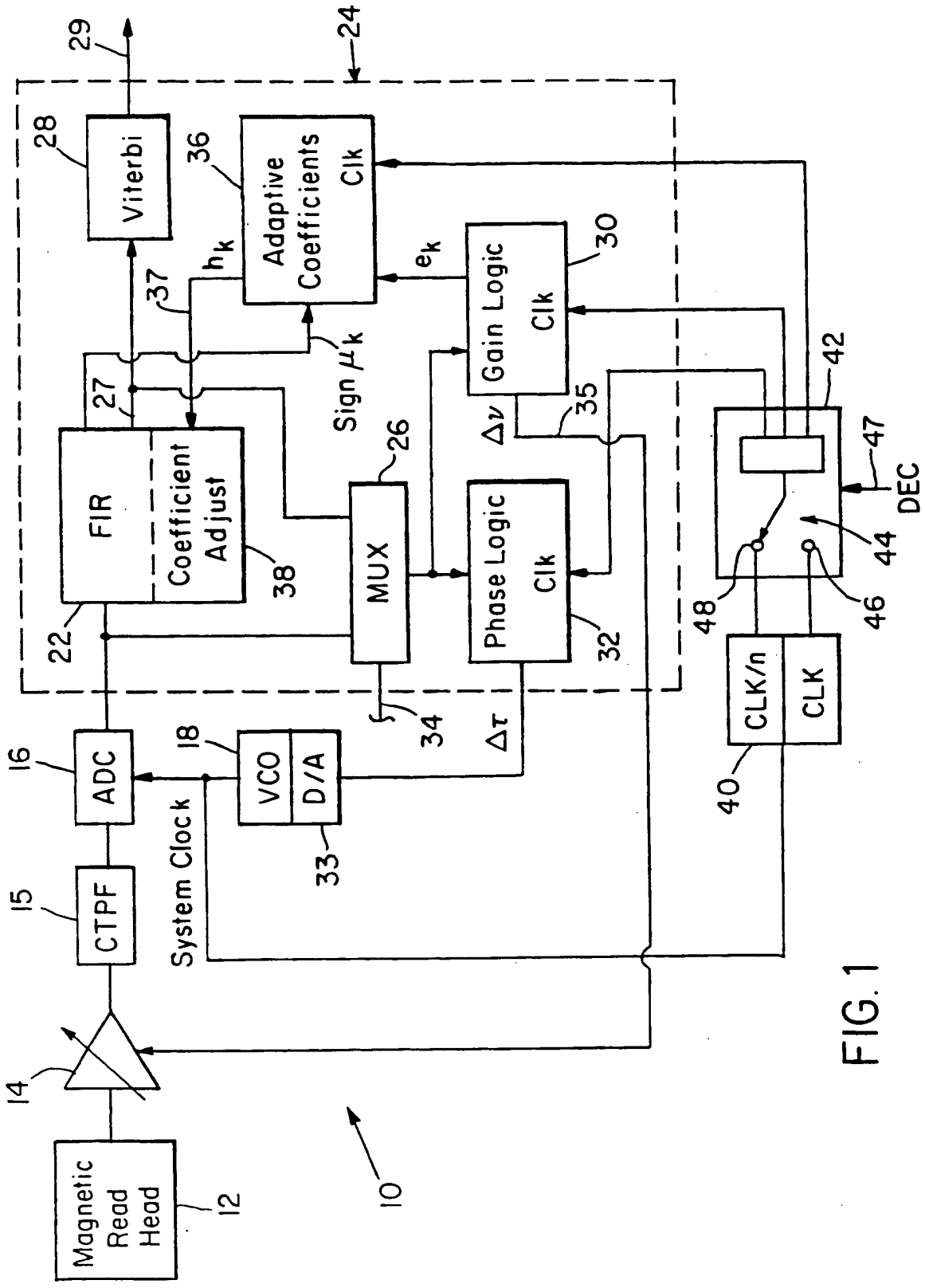
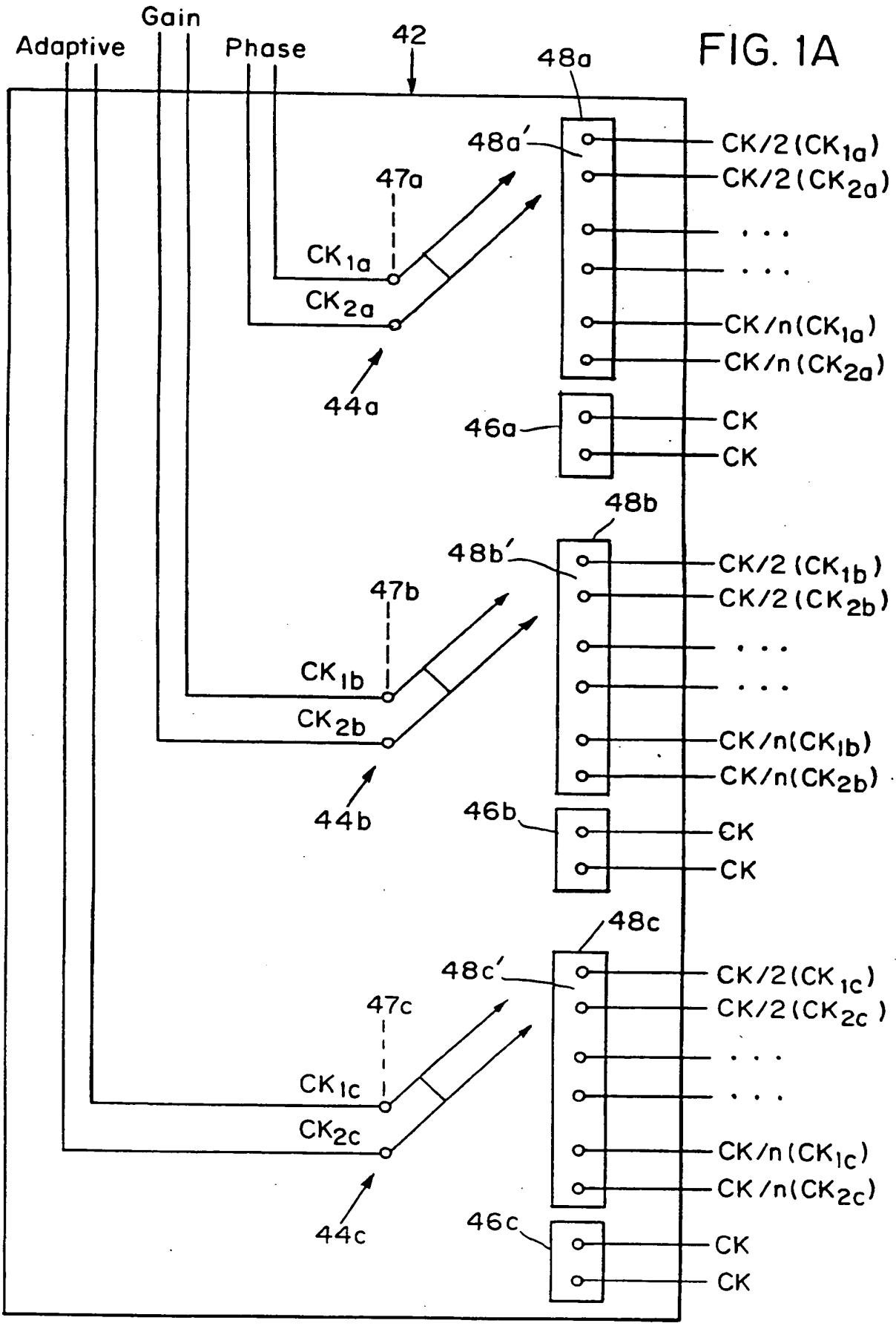



FIG. 1

FIG. 1A



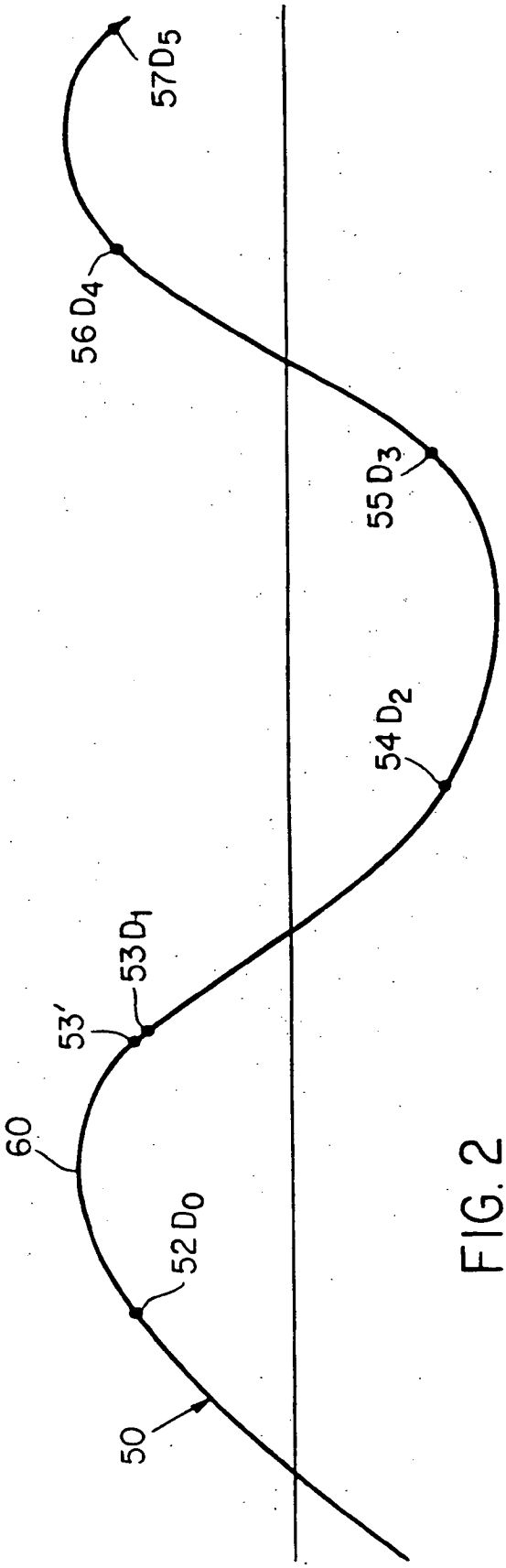



FIG. 2

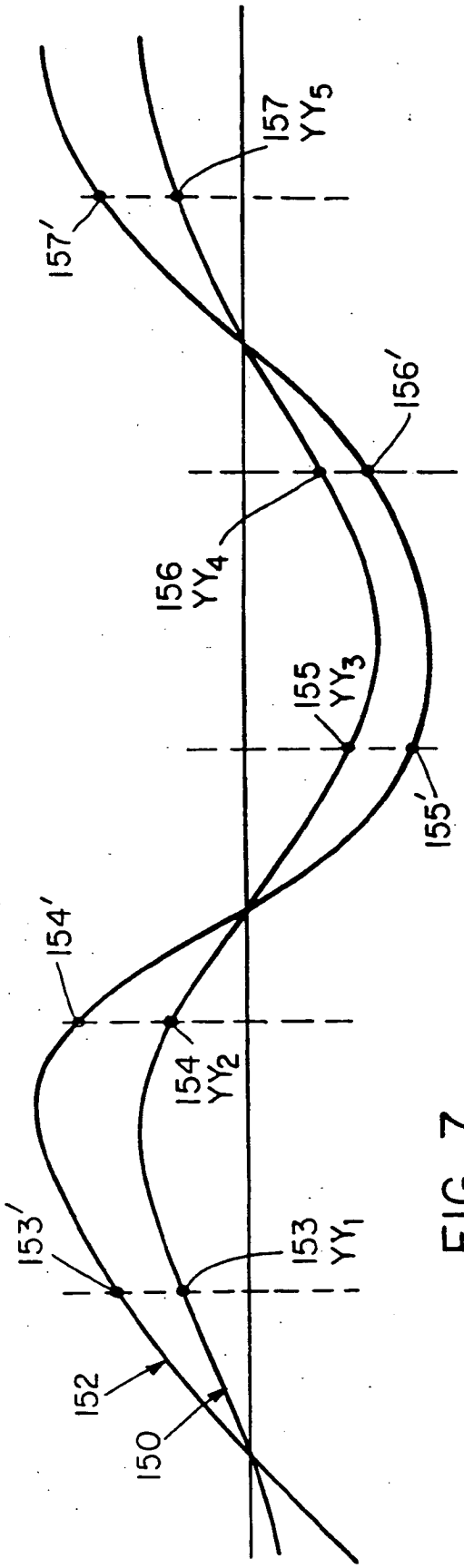



FIG. 7

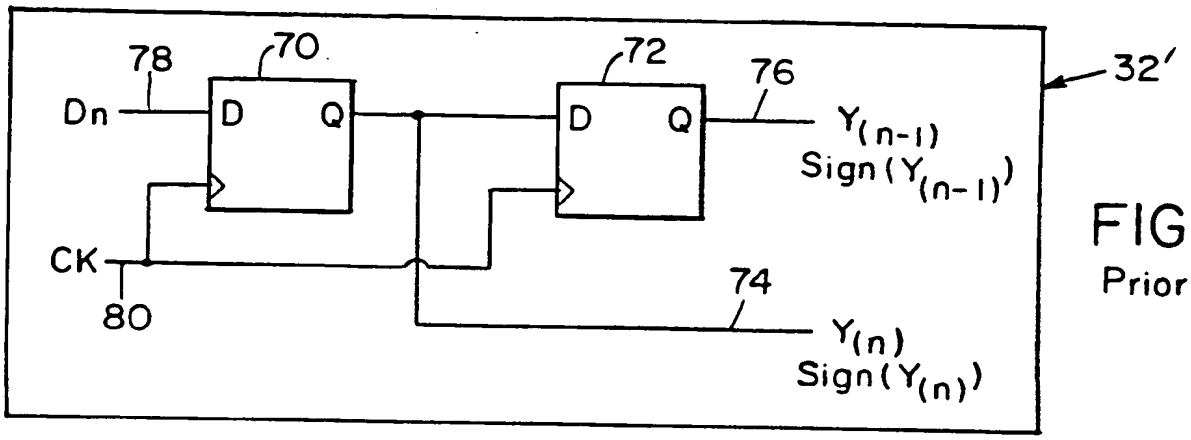



FIG. 3
Prior Art

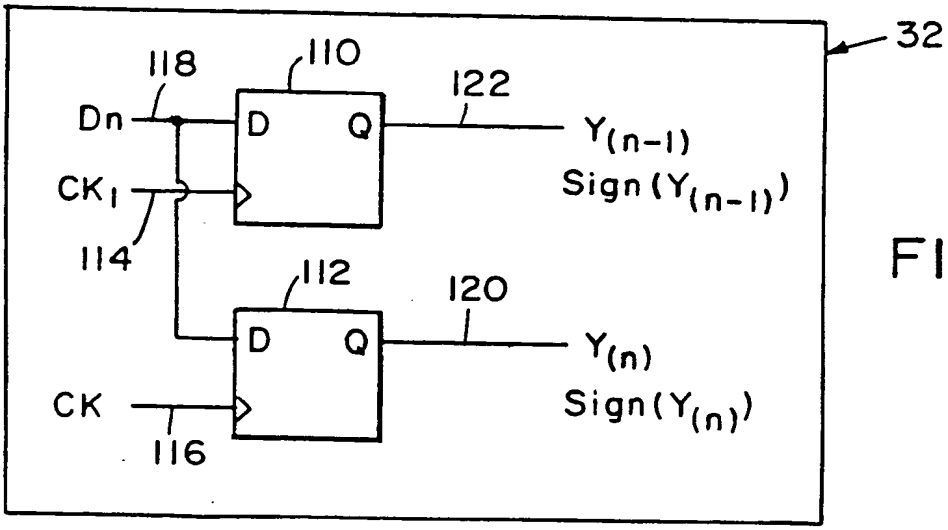



FIG. 5

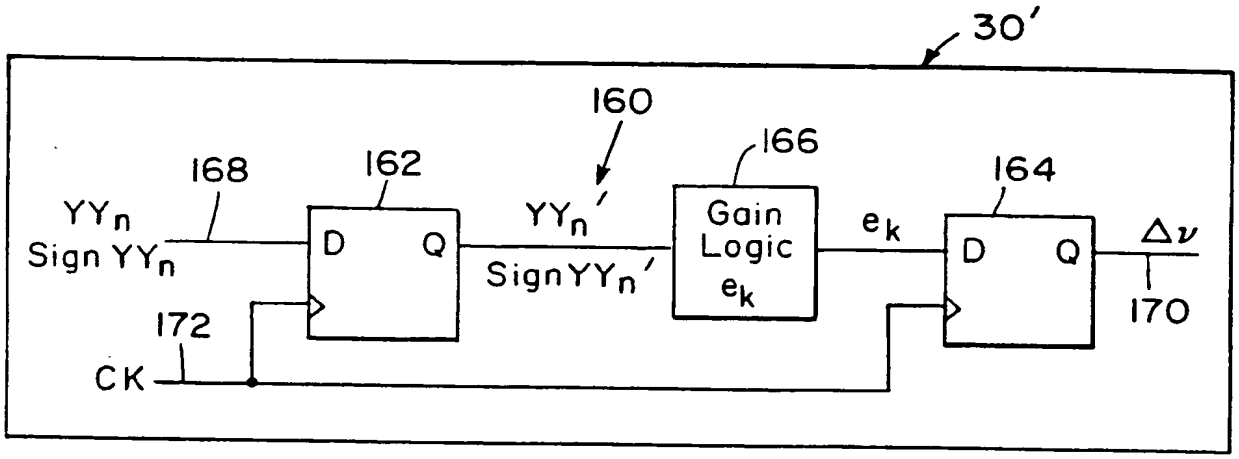



FIG. 8
Prior Art

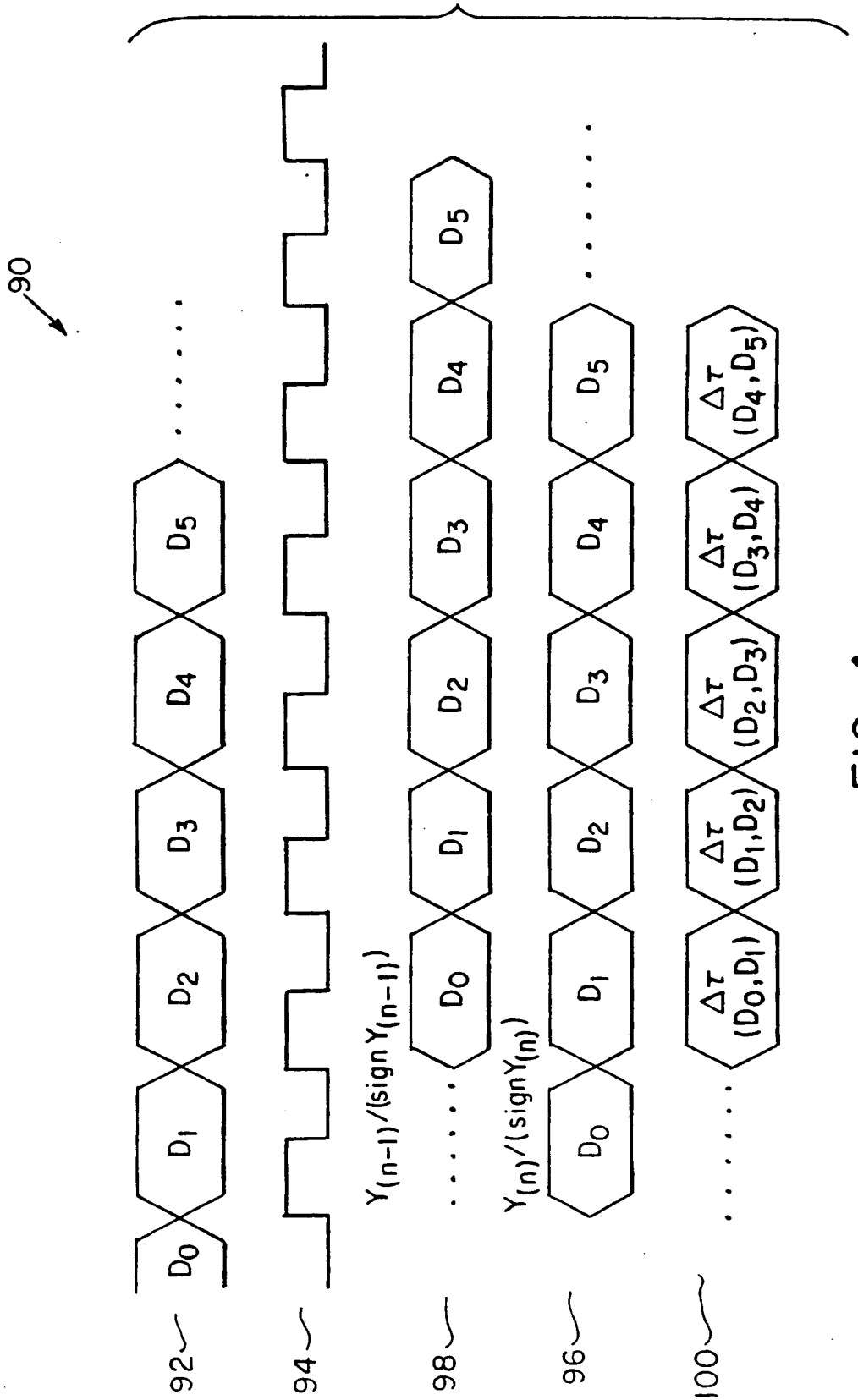



FIG. 4

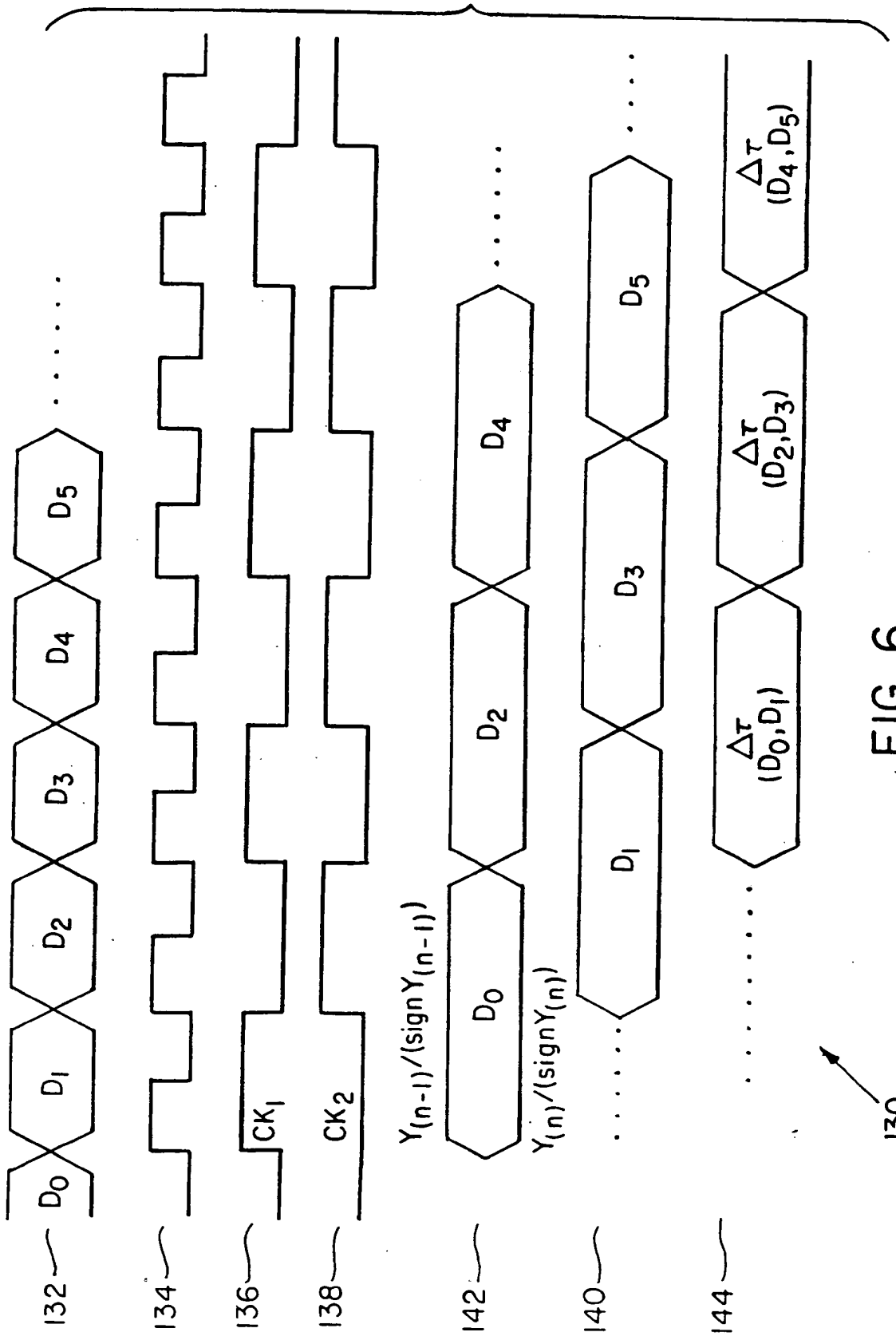



FIG. 6

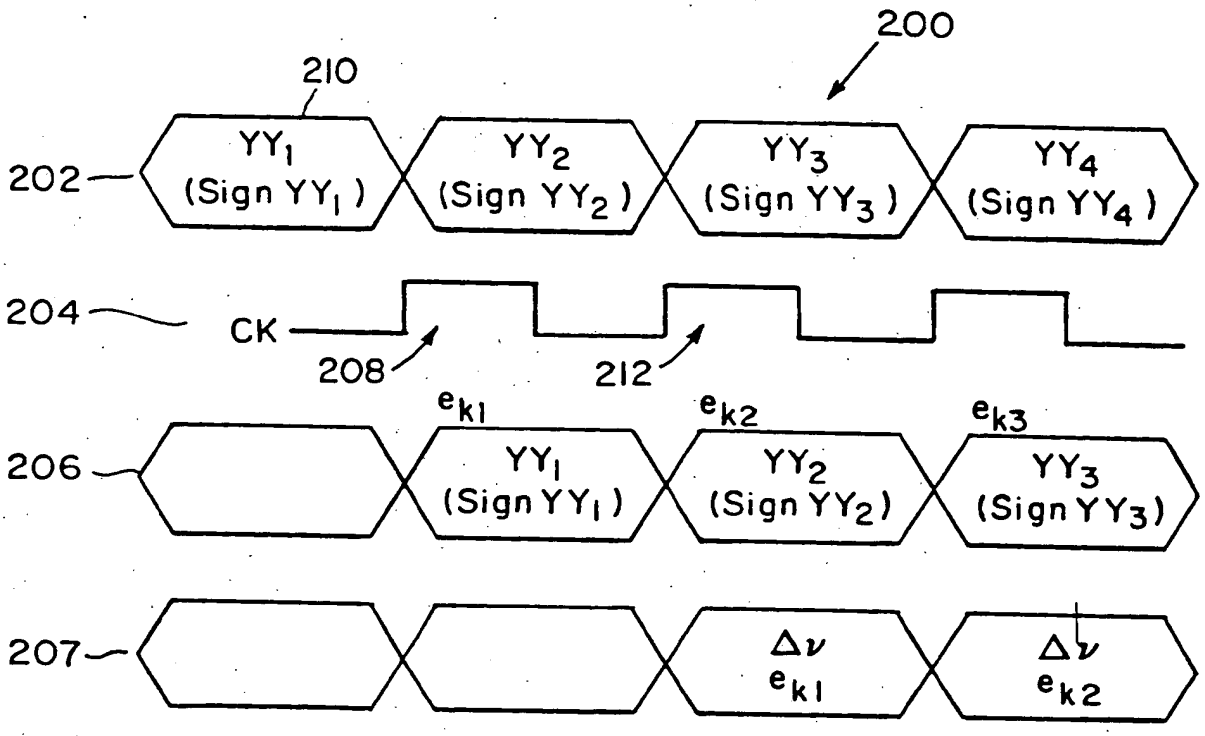



FIG. 9

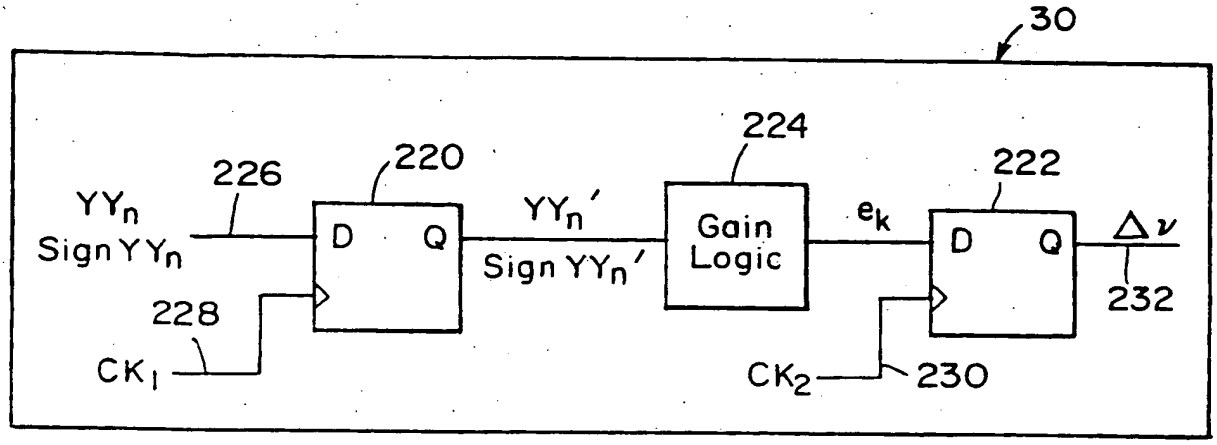



FIG. 10

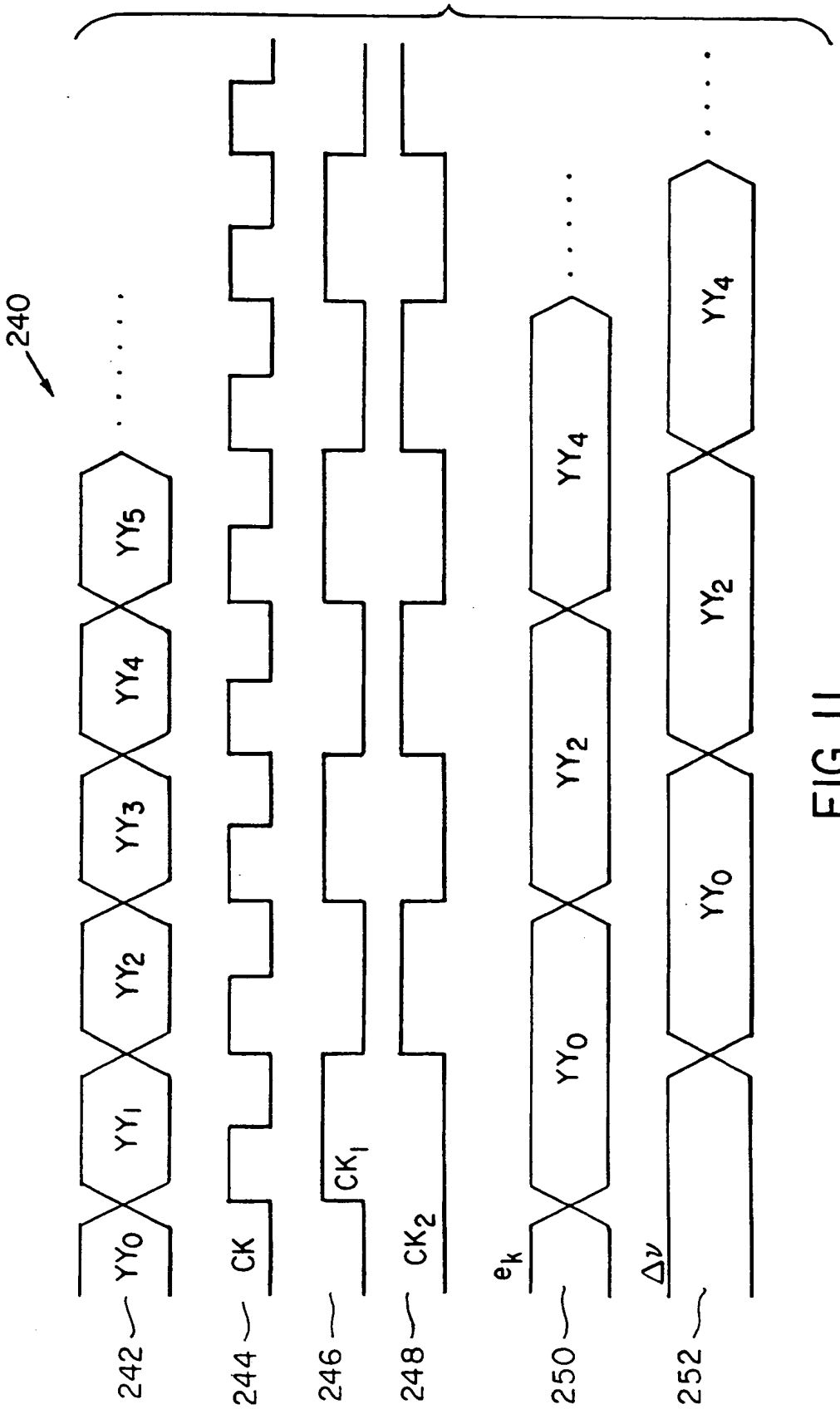



FIG. 11

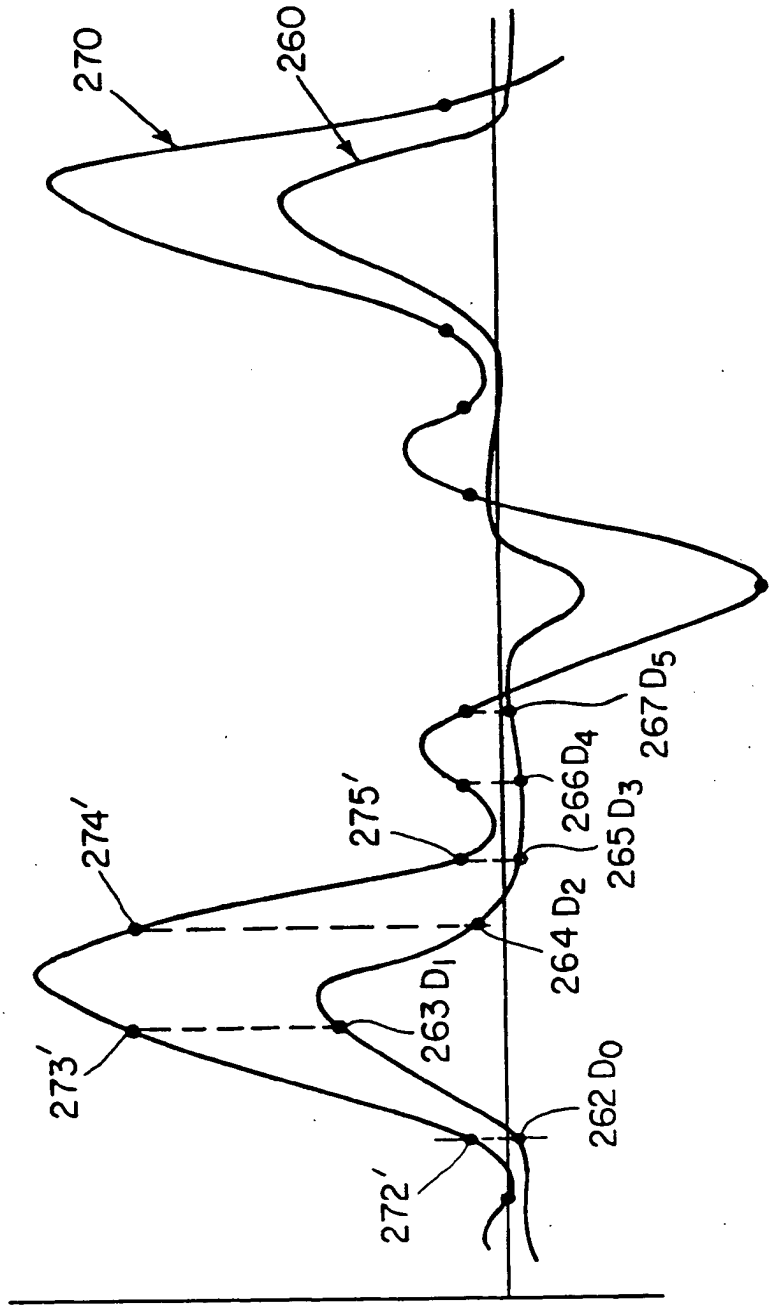



FIG. 12

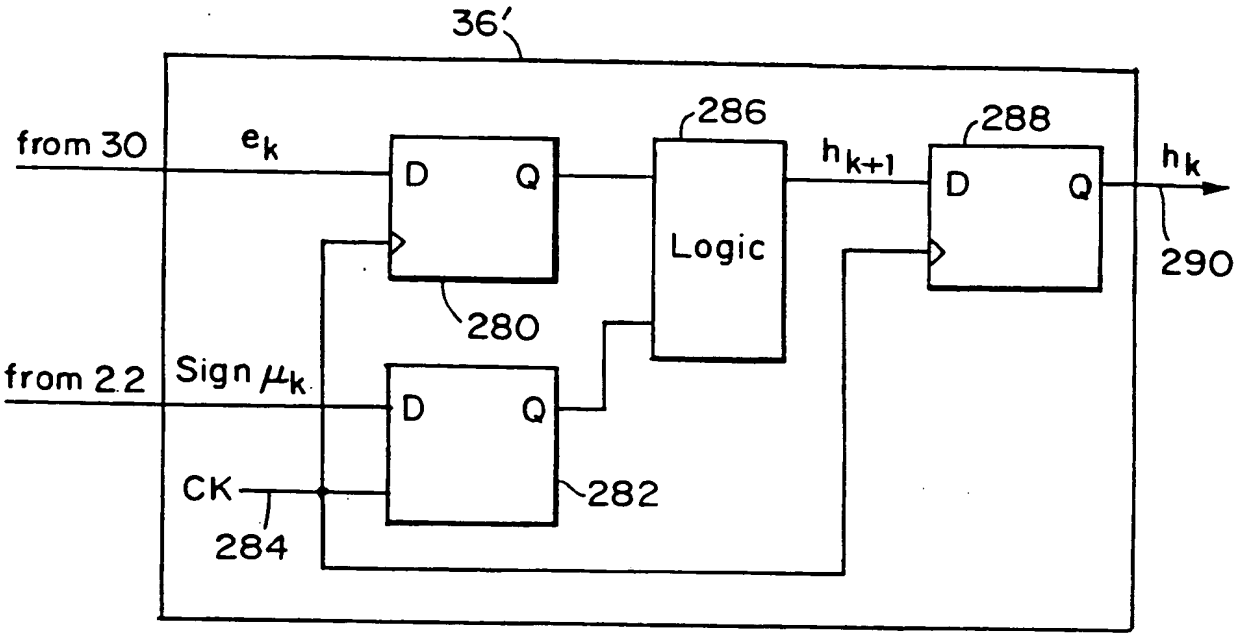



FIG. 13
Prior Art

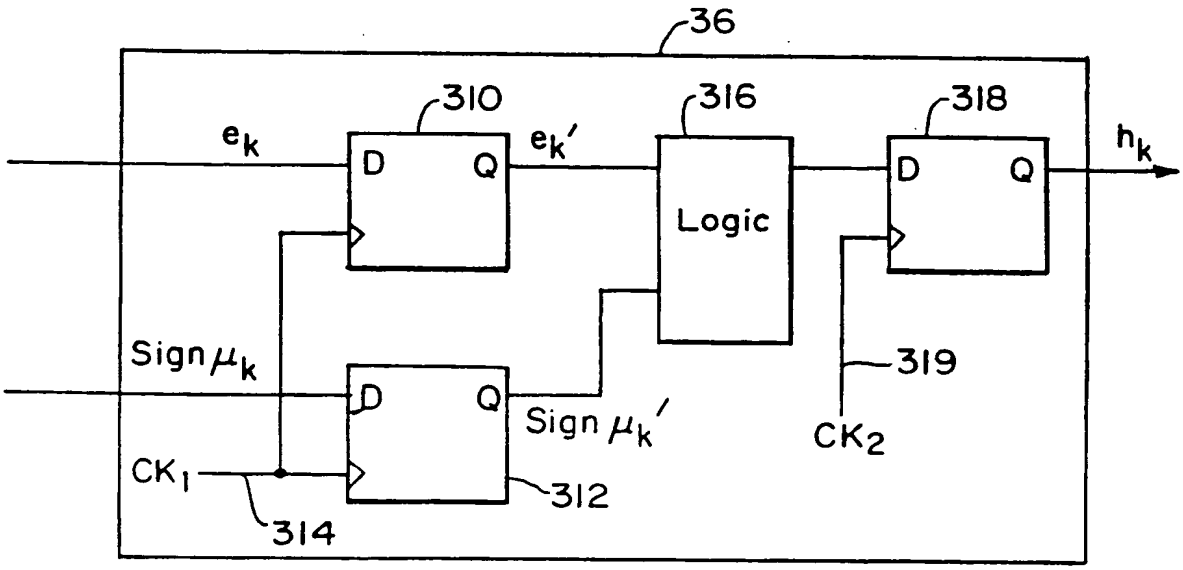



FIG. 15

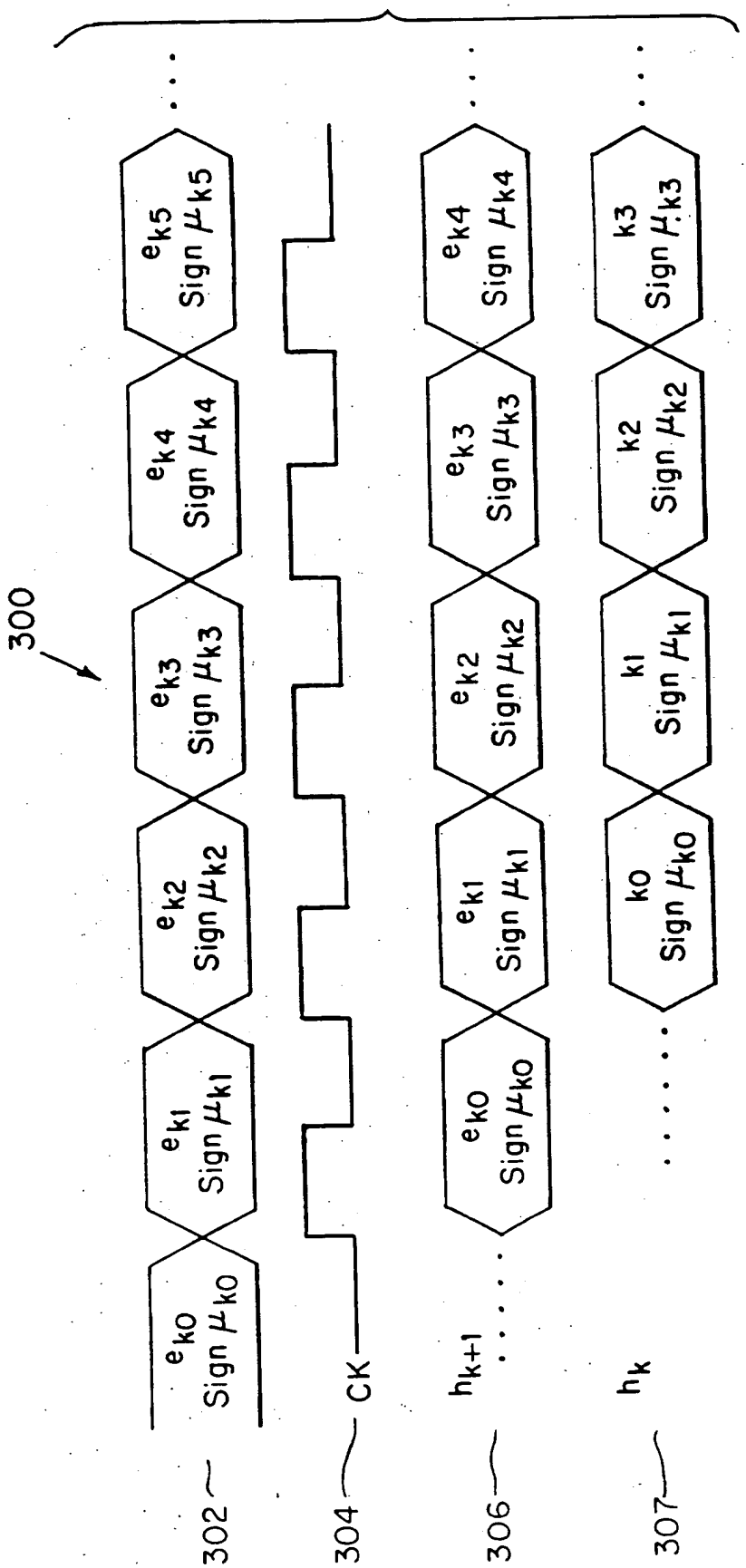



FIG. 14

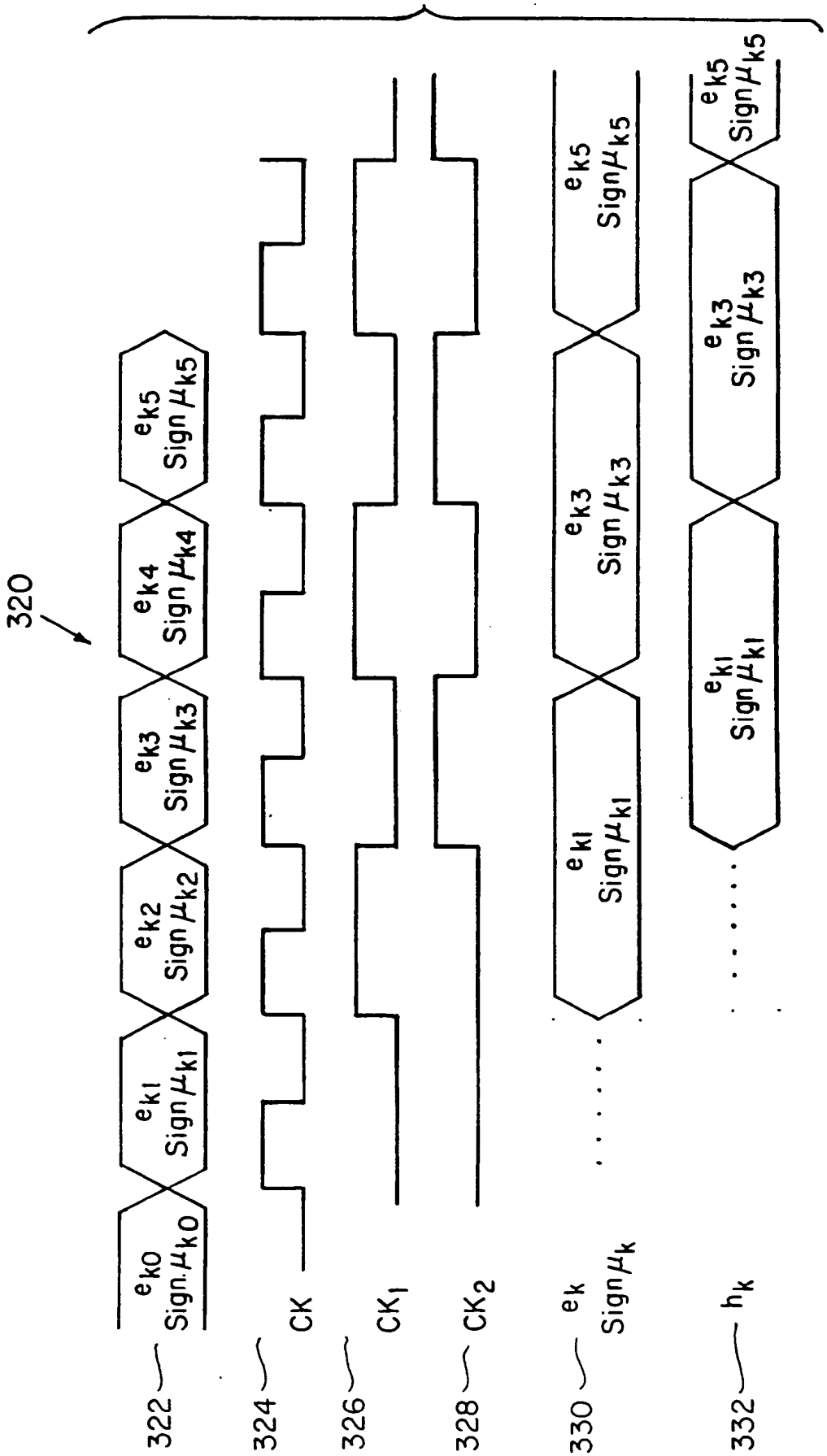



FIG. 16

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/02743

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(6) :H03M 13/00
US CL : 375/341

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | IEEE Journal of Solid-State Circuits, Vol.29, No.12, December 1994, Uehara et al., " A 100 MHz A/D Interface for PRML Magnetic Disk Read Channels" section III and figure 6. | 1-2, 4 |
| Y | IEEE Journal on Selected Areas in Communications, Vol.10, No. 1, January 1992, Cideciyan et al., " A PRML System for Digital Magnetic Recording" pages 38-56 | 1-6 |
| Y | IEEE International Solid-State Circuits Conference, 1995, Digest of Technical Papers, Richetta et al.," A 16MB/s PRML Read/Write Data Channel" pages 78-79 | 1-6 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

| | | | |
|---|---|---|---|
| * | Special categories of cited documents: | "T" | later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention |
| "A" | document defining the general state of the art which is not considered to be part of particular relevance | "X" | document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone |
| "E" | earlier document published on or after the international filing date | "Y" | document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art |
| "L" | document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) | "&" | document member of the same patent family |
| "O" | document referring to an oral disclosure, use, exhibition or other means | | |
| "P" | document published prior to the international filing date but later than the priority date claimed | | |

| | |
|---|---|
| Date of the actual completion of the international search<br>19 APRIL 1996 | Date of mailing of the international search report<br>07 MAY 1996 |
| Name and mailing address of the ISA/US<br>Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231<br>Facsimile No. (703) 305-3230 | Authorized officer<br>BRYAN WEBSTER<br>Telephone No. (703) 305-4700 |

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